Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NOBORU TAKIZAWA

Appeal No. 95-3091
Application 08/093,311[1]

HEARD: May 4, 1998

Before KRASS, BARRETT and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-5, the only claims in the application. No claim has been allowed.

References relied on by the Examiner

McCullough et al. (McCullough)	4,979,054	Dec. 18, 1990
Yoshimura et al. (Yoshimura)	5,063,453	Nov. 5, 1991

The Rejections on Appeal

Claims 1-5 stand finally rejected under 35 U.S.C. §

[1] Application for patent filed February 2, 1993.

103 as being unpatentable over Yoshimura and McCullough (Paper No. 6, at 2).

The Invention

The invention is directed to a disk drive wherein the stored data contains an error correction code added thereto before writing of the data onto the disk. The number of bits in the error correction code is selected in accordance with a selection signal generated by a circuit which is responsive to a track address indicating a location on the recording medium. Claim 1 is the only independent claim and is reproduced below:

1. A disk drive apparatus in which an error correction code is added to data before it is written to a recording disk medium, comprising:

a selection signal generation circuit responsive to a track address indicating an access location on the medium, for generating a selection signal to be used for selecting a number of bits of the error correction code; and

a read-write circuit for performing a data read or write operation to the medium while selecting the number of bits of the error correction code in accordance with the selection signal.

Opinion

We do not sustain the rejection of claims 1-5.

The appellant argues that neither Yoshimura nor McCullough contains any teaching "of varying the error correction code [number of bits therein] according to the track address at which the data is to be recorded" (Br. at 13). The independent claim, however, does not actually require the number of bits in the error correction code to be varied. The independent claim requires only that the selection of the number of bits be based on the track address. Thus, the appellant's argument is more appropriately regarded as this: As far as the applied prior art is concerned, the number of bits in the error correction code is not selected based on the track address of the location of the data to be stored. In our view, this argument has merit.

Yoshimura discloses a digital signal recording apparatus including an error-correction-code adding circuit for adding an error correction code to the data to be written to the recording medium, a videotape. The examiner acknowledges that Yoshimura does not disclose the claimed selection signal generating circuit as is recited in claim 1 (answer at 4).

The appellant correctly points out (Br. at 7) that Yoshimura does not describe the number of bits used in the

error correction code or imply that codes with different numbers of bits should be used. The appellant also correctly notes (Br. at 7) that because the recording rate does not vary with position in a **tape** recording system, in Yoshimura "there is no variation in the probability of error which is dependent on the location of the recording address" (as there would be in a disk drive storage system as claimed). Nothing in Yoshimura would have reasonably suggested the generation of a selection signal based on the location of the track address on a disk, which selection signal selects the number of bits in the error correction code.

The examiner's reliance on McCullough to show the feature missing from Yoshimura is also misplaced and without merit. As is correctly noted by the appellant (Br. at 7-11), McCullough discloses that the number of bits used for the error-correction-code is 56, or alternatively, 32 (column 22, lines 12-14; column 23, lines 22-29). The appellant is also correct that the examiner has identified nothing in McCullough

which reasonably would have suggested that the selection of the number of bits in the error-correction-code is made based on the track address of the data sector to be written in. Indeed, if anything, McCullough appears to suggest the contrary, that the same length error-correction-code is always used regardless of the track address. In that connection, note the following text in column 19, lines 19-23, of McCullough:

> In the present embodiment only RLL (2,7) encoding is utilized and the disk controller 182 is programmed to perform 56-bit ECC [error correction code] on the data field and 16-bit CRC on the sector identification but could be programmed to perform otherwise if desired.

The examiner has pointed to nothing to indicate that the programming as described in the above-quoted text is on a track by track basis. The more plausible reading of McCullough is that the length of the code is uniform for all data sectors in all tracks, even though it can be either 56 bits or 32 bits long.

Neither Yoshimura nor McCullough discloses or

reason- ably suggests the key feature of the appellant's invention, that the number of bits in the error-correction-code is selected based on the track address of the location of data storage. No reason has been set forth by the examiner as to why the combined teachings of Yoshimura and McCullough would have suggested that which neither one alone would have suggested. The two references do not combine in any reasonable manner to suggest that the num- ber of bits used in the error-correction-code should be selected based on the track address of the location to be written in.

On pages 4-6 of the examiner's answer, the reasons provided in the final Office action as to why the examiner con- cludes that it would have been obvious to one with ordinary skill in the art to vary the number of bits in the error-correction-code based on the track address of the location to be written in

is reiterated. It is explained that because the recordings are more dense on the inner tracks and less dense on the outer tracks, the probability of recording error is higher on the inner tracks and lower on the outer tracks. For that reason, the examiner concludes that it would have been prima facie

obvious to one with ordinary skill in the art to select a shorter error-correction-code for the outer tracks and a longer error-correction-code for the inner tracks.

The problem with the examiner's position, however, is that the explanation largely coincides with the appellant's reasons underlying the claimed invention and does not stem from either Yoshimura, McCullough, or a combination thereof. On this record and based on the parts of the cited references discussed by the examiner, we conclude that the examiner's rationale is gleaned solely from hindsight based on the appellant's own disclosure. That is improper. The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor. Para-Ordnance Mfg. Inc. v. SGS

Importers Int'l Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), cert. denied, 117 S.Ct. 80 (1996). In our view, the reasoning of the examiner is at a level beyond that which can be said to have been necessarily possessed by one with ordinary skill in the art without explicit or implied suggestion from the prior art.

Claim 2, which depends from claim 1, further recites that the number of bits is selected from a plurality of numbers
that are predetermined for respective "groups" of tracks on the medium. On this record, suggestion for such a feature also derives solely from the appellant's own disclosure. Claim 3, which depends from claim 2, recites that the number of bits decreases as the group of tracks approaches an outermost track of the medium.

Claim 4, which depends from claim 1, further recites collation of the track address to a detection value which is predetermined according to an inspection result indicating the possibility of error for the corresponding track. On this record, suggestion for such a feature also derives solely from the appellant's own disclosure. Claim 5 depends from claim 1.

For the foregoing reasons, we do not sustain the obviousness rejection of claims 1-5.

Conclusion

The rejection of claims 1-5 under 35 U.S.C. § 103 as being unpatentable over Yoshimura and McCullough is reversed.

REVERSED

ERROL A. KRASS)
Administrative Patent Judge)
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) BOARD OF PATENT
LEE E. BARRETT) APPEALS AND
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